IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A differential amplifier circuit comprising:

a first differential amplifier for receiving a pair of differential input signals to generate a first output;

a second differential amplifier for receiving said pair of differential input signals to generate a second output;

a summing circuit for summing said first output of said first differential amplifier and said second output of said second differential amplifier to provide a common output for said differential amplifier circuit; and

a reference voltage generation circuit for providing a reference voltage signal to said summing circuit, wherein said reference voltage generation circuit is a differential amplifier, wherein said summing circuit includes an n-channel transistor pair, wherein a first transistor of said n-channel transistor pair receives said voltage reference signal from said reference voltage generation circuit, wherein a second transistor of said n-channel transistor pair receives combined output signals from said first output of said first differential amplifier and said second output of said second differential amplifier.

2. (original) The differential amplifier circuit of Claim 1, wherein said first differential amplifier is an n-channel differential amplifier.

3. (original) The differential amplifier circuit of Claim 2, wherein said first differential amplifier includes a pair of n-channel transistors for receiving said pair of differential input signals, respectively.

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4. (original) The differential amplifier circuit of Claim 1, wherein said second differential amplifier is a p-channel differential amplifier.

5. (original) The differential amplifier circuit of Claim 1, wherein said second differential amplifier includes a pair of p-channel transistors for receiving said pair of differential input signals, respectively.

6. (original) The differential amplifier circuit of Claim 1, wherein said summing circuit is an n-channel differential amplifier.

7. cancelled

8. (previously presented) The differential amplifier circuit of Claim 1, wherein said reference voltage generation circuit is a p-channel differential amplifier.

9. (previously presented) The differential amplifier circuit of Claim 8, wherein said reference voltage generation circuit receives an active low ENABLE_P signal.

10. (original) The differential amplifier circuit of Claim 1, wherein said first and second differential amplifiers receive an active low ENABLE_N signal.

11. (original) The differential amplifier circuit of Claim 10, wherein said summing circuit receives an active low ENABLE_P signal.

12. (original) The differential amplifier circuit of Claim 11, wherein said summing circuit includes a clamp device to hold said common output high when said ENABLE_P signal is low.

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13. (original) The differential amplifier circuit of Claim 1, wherein said first differential amplifier receives a gate control voltage V_{CMN} to control the current through an n-channel transistor within said first differential amplifier in a consistent and predictable manner using a current mirror technique.

14. (original) The differential amplifier circuit of Claim 1, wherein said second differential amplifier receives a gate control voltage V_{CMP} to control the current through a p-channel transistor within said second differential amplifier in a consistent and predictable manner using a current mirror technique.

15. (original) The differential amplifier circuit of Claim 1, wherein said summing circuit receives a gate control voltage V_{CMN} to control the current through an n-channel transistor within said summing circuit in a consistent and predictable manner using a current mirror technique.

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